LISTING OF CLAIMS:

The following listing of claims replaces all previous versions, and listings of claims in the present application.

Please cancel claims 2-7 without prejudice or disclaimer.

1. – 7. (Canceled)

8. (Previously presented) A shift clock signal generating apparatus for generating a shift clock signal having a prescribed phase difference from a reference clock signal, comprising:

a delay line receiving the reference clock signal and including a plurality of unit delay elements connected in cascade, wherein each of the unit delay elements provides a prescribed signal delay time, and the reference clock signal propagates in the delay line while being successively delayed by the unit delay elements;

a shift clock signal output path;

a group of switches having first ends connected with output terminals of the unit delay elements respectively, and second ends connected with the shift clock signal output path, wherein when specified one among the switches is in its on position, a delayed clock signal which results from delaying the reference clock signal by a prescribed time interval is transmitted via the specified switch to the shift clock signal output path as the shift clock signal; and

switch controlling means for determining the specified one among the switches on the basis of data representing a phase difference of the shift clock signal from the reference clock signal, and for setting the specified switch in its on position,

wherein the switch controlling means operates for determining the specified one among the switches on the basis of period data and ratio data, the period data representing a numeric value of a period of the reference clock signal while a time resolution is given by the prescribed signal delay time provided by each of the unit delay elements, the ratio data representing a ratio between a delay time of the shift clock signal relative to the reference clock signal and the period of the reference clock signal.

9. (Original) A shift clock signal generating apparatus as recited in claim 8, wherein the ratio represented by the ratio data is equal to y/(x+l), and "x" denotes a predetermined natural number and "y" denotes a natural number in a range of "1" to "x".

10. (Original) A shift clock signal generating apparatus as recited in claim 9, further comprising:

a ring delay line including a plurality of unit delay elements connected in a closed loop and being equal in characteristics to the unit delay elements in the previously-mentioned delay line, wherein a pulse signal circulates through the ring delay line while being delayed by the unit delay elements; and

time A/D converting means for counting a number of times the pulse signal goes round the ring delay line, for generating the period data in response to the counted number of times, and for feeding the period data to the switch controlling means.

11. (Original) A shift clock signal generating apparatus as recited in claim 8, further comprising a digitally controlled oscillation circuit for outputting a signal having a period controllable while a time resolution is given by the prescribed signal delay time provided by each of the unit delay elements, the digitally controlled oscillation circuit using control data in controlling the period of the signal outputted therefrom, the delay line receiving the signal outputted from the digitally controlled oscillation circuit as the reference clock signal, the switch controlling means operating for using the control data as the period data.

12. (Original) A shift clock signal generating apparatus as recited in claim 8, further comprising a digitally controlled oscillation circuit for outputting a signal having a period controllable while a time resolution is given by the prescribed signal delay time provided by each of the unit delay elements, the digitally controlled oscillation circuit using control data in controlling the period of the signal outputted therefrom, and a frequency divider circuit for dividing a frequency of the signal outputted from the digitally controlled oscillation circuit to generate the reference clock signal having a duty cycle of 50%, the delay line receiving the reference clock signal generated by the frequency divider circuit, the switch controlling means operating for doubling a period represented by the control data to calculate the period of the reference clock signal and for generating the period data in accordance with the calculated period.

13. (Original) A shift clock signal generating apparatus as recited in claim 11, wherein the digitally controlled oscillation circuit includes:

a ring delay line including a plurality of unit delay elements connected in a closed loop and being equal in characteristics to the unit delay elements in the previously-mentioned delay

line, wherein a pulse signal circulates through the ring delay line while being delayed by the unit delay elements;

time A/D converting means for counting a number of times the pulse signal goes round the ring delay line, for generating the period data in response to the counted number of times, and for outputting the period data; dividing means for dividing a value of the period data outputted from the time A/D converting means by a preset number to generate the control data; and

signal outputting means for comparing a value of the control data and a number of times the pulse signal passes through a unit delay element in the ring delay line, and for outputting a prescribed-pulsewidth signal each time the value of the control data and the number of times become equal to each other.

14. – 22. (Canceled)

23. (Previously presented) A shift clock signal generating apparatus as recited in claim 8, further comprising a plurality of second delay lines each being equal in structure to the delay line, a plurality of second groups of switches each being equal in structure to the group of switches, a plurality of second shift clock signal output paths each being equal in structure to the shift clock signal output path, and a plurality of second switch controlling means each being equal in structure to the switch controlling means to generate shift clock signals having prescribed phase differences from the reference clock signal, the prescribed phase differences being different from each other, wherein a number of the second delay lines, a number of the second groups of switches, a number of the second shift clock signal output paths, and a number of the second switch controlling means correspond to a number of the shift clock signals.

24. (Previously presented) A shift clock signal generating apparatus as recited in claim 8, further comprising a plurality of second groups of switches each being equal in structure to the group of switches, a plurality of second shift clock signal output paths each being equal in structure to the shift clock signal output path, and a plurality of second switch controlling means each being equal in structure to the switch controlling means to generate shift clock signals having prescribed phase differences from the reference clock signal, the prescribed phase differences being different from each other, wherein first ends of the switches in each of the second groups are connected with the output terminals of the plurality of unit delay elements respectively, and wherein a number of the second groups of switches, a number of the second shift clock signal output paths, and a number of the second switch controlling means correspond to a number of the shift clock signals.

25. (Previously presented) A shift clock signal generating apparatus as recited in claim 24, wherein the second groups of switches are connected with the output terminals of ones among the unit delay elements in correspondence with the prescribed phase differences of respective shift clock signals from the reference clock signal.

26. (Previously presented) A shift clock signal generating apparatus as recited in claim 25, wherein the unit delay elements are separated into groups having a number equal to a number of the shift clock signals, and the second groups of switches are connected respectively with unit delay elements in the corresponding groups of unit delay elements.

27. (Previously presented) A shift clock signal generating apparatus as recited in claim 8, further comprising a reference clock signal output path for outputting the reference clock signal.

28. (Previously presented) A shift clock signal generating apparatus as recited in claim 8, wherein each of the unit delay elements includes a gate circuit for providing the prescribed signal delay time.